**Code No: IT14213**

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (Autonomous)**

**BE (IT) II Yr I Sem (Main) Examination Dec 2014/Jan 2015**

**DIGITAL ELECTRONICS & LOGIC DESIGN**

**Time: 3 Hours Max Marks:75**

**Note:** Answer all questions from **Section-A** at one place in the same order

Answer any **five** questions from **Section-B**

**SECTION - A (25 Marks)**

1. Simplify using DeMorgan’s theorem f=( a(b+c’))’ (2)

2. Implement XOR gate using four NAND gates (3)

3. What is the advantage of LUT? Give one example. (3)

4. Write a VHDL code for a 2:1 MUX using behavioural modeling (3)

5. Write the truth table and excitation table of a JK flip-flop (3)

6. Write a VHDL code for a D flip-flop (2)

7. Draw the state diagram for detecting the sequence ‘01’ (3)

8. Determine the number of flip-flops required when a FSM uses 100 states (2)

9. Define clock skew (2)

10. Define dynamic hazard (2)

**SECTION - B (50 Marks)**

11. Simplify using K-map

(i) ∑ m(0,1,3,5,8,10,12) + D (7, 11,14) (4)

(ii) Implement the above logic using logic gates (3)

(iii) Write a VHDL code for implementing the above circuit by instantiating logic

gates (3)

12. Prove the following equations using the Boolean algebraic theorems:

(i) A + A’B + AB’ = A + B (2)

(ii) A’BC + A B’ C + ABC’ + ABC = AB + BC + AC (2)

(iii) Implement the above simplified logic functions using 2-input LUT and draw the

internal structure of a 2-input LUT (6) **PTO**

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13. (a) Draw the circuit of a 3-bit up/down counter and explain its operation along with the

waveforms at the output of each flip-flop (5)

(b) Draw a 2-bit ring counter and explain its operation with the help of waveforms (5)

14. (a) Design an FSM circuit for detecting the sequence ‘111’. It has one input and one

output. The output should become ‘1’ whenever the above sequence is detected.(6)

(b) Write the VHDL code to implement the above FSM circuit (4)

15. (a) Write the pseudo - code for multiplication. Draw the data path circuit for

the multiplier (5)

(b) Design an asynchronous sequential circuit for the problem 14.(a) (5)

16. (a) Draw the internal architecture of FPGA and Explain. (5)

(b) Construct a 4-bit right shift register with parallel load facility (5)

17. Write short notes on the following

(a) Master-slave flip-flop (5)

(b) ASM chart for sort operation (5)